**CLAIM AMENDMENTS** 

Claim 52 (previously presented) A circuit comprising:

a first delay line having a first set of output taps and a first input terminal for receiving a

first signal;

a second delay line having a second set of output taps and second input terminal for

receiving a second signal;

a first multiplexor coupled to the first set of output taps, the first multiplexor providing a

third signal to a first storage device;

a second multiplexor coupled to the second set of output taps, the second multiplexor

providing a fourth signal to the first storage device; and

a control circuit for comparing a fifth signal to an input clock signal to generate a first

control signal, wherein the fifth signal corresponds with an output signal of the first storage

device.

Claim 53 (previously presented) The circuit of claim 52, wherein the first and

second signals are complementary to one another.

Claim 54 (currently amended) The circuit of claim 52, further comprising:

a third multiplexor coupled with the first set of output taps, wherein the third multiplexor

provides a sixth signal to a first interpolator circuit;

a fourth multiplexor coupled with the second set of output taps, wherein the fourth

multiplexor provides a seventh signal to the first interpolator circuit;

a fifth multiplexor coupled with the first set of output taps, wherein the fifth multiplexor

provides an eighth signal to a second interpolator circuit;

a sixth multiplexor coupled with the second set of output taps, wherein the sixth

multiplexor provides a ninth signal to the second interpolator circuit;

wherein the first interpolator provides a tenth signal to a second storage device;

the second interpolator provides an eleventh signal to the second the second

storage device; and

the second storage device provides a twelfth signal that operates as a quadrature

output clock signal; and

a second control circuit that provides a second control signal, a third control signal, a

fourth control signal, and a fifth control signal, respectively, to the third multiplexor, the fourth

multiplexor, the fifth multiplexor, and the sixth multiplexor.

(previously presented) The circuit of claim 54, further comprising a flip-Claim 55

flop for generating a test signal, the flip-flop having a data input terminal coupled with the third

multiplexor to receive the sixth signal and a clock input terminal coupled with the fourth

multiplexor to receive the seventh signal, wherein

the second control circuit receives the first control signal and the test signal and generates

the second control signal and the fifth control signal by offsetting the first control signal by a

selected offset value in a first direction relative to the magnitude of the first control signal and

generates the third control signal and the fourth control signal by offsetting the first control signal

by the selected offset value in a second direction that is opposite to the first direction, where the

3

McDonnell Boehnen Hulbert & Berghoff LLP 300 South Wacker Drive Chicago, Illinois 60606

selected offset value is selected by starting with a first value and successively changing the

selected offset value until the test signal changes value.

Claim 56 (previously presented) The circuit of claim 52, wherein a rising edge of the

fifth signal, which corresponds to the output signal of the first storage device, corresponds to a

rising edge of the third signal provided by the first multiplexor and a falling edge of the fifth

signal corresponds with a rising edge of the fourth signal provided by the second multiplexor.

Claim 57 (previously presented) The circuit of claim 52, wherein the first control

circuit includes a detection circuit for determining a phase difference between the fifth signal,

which corresponds to the output signal of the first storage device, and the input clock signal.

Claim 58 (previously presented) The circuit of claim 53, wherein the first and

second delay lines each include power control circuitry for selectively powering off one or more

delay elements of the first and second delay lines.

Claim 59 (previously presented) The circuit of claim 58, wherein the control circuit

provides a power control signal to the first and second delay lines, wherein the power control

circuitry selectively powers off the one or more delay elements in correspondence with the power

control signal.

Claim 60 (previously presented) The circuit of claim 52, further comprising a phase

splitter for receiving a reference clock signal and generating the first and second signals, the first

signal being in phase with the reference clock and the second signal being out of phase with the

reference clock; and

wherein the first storage device comprises a reset-able latch device; and

the first control circuit comprises:

a phase detector for receiving the fifth signal, which corresponds to the output

signal of the reset-able latch device, and the input clock signal, and generating a

difference signal that indicates the phase relationship between the fifth signal and the

input clock signal; and

a controller for receiving the difference signal and generating the first control

signal, the controller being responsive to the difference signal so as to phase align the

fifth signal and the input clock signal using the control signal to select respective output

taps of the first and second sets of output taps.

Claim 61 (currently amended) A circuit comprising:

a first delay line having a first set of output taps and a first input terminal for receiving a

first signal;

a second delay line having a second set of output taps and a second input terminal for

receiving a second signal;

a first multiplexor coupled to the first set of output taps, the first multiplexor providing a

5

third signal to a first storage device;

McDonnell Boehnen Hulbert & Berghoff LLP 300 South Wacker Drive Chicago, Illinois 60606

(312) 913-0001

a second multiplexor coupled to the second set of output taps, the second multiplexor

providing a fourth signal to the first storage device;

a control circuit for comparing a fifth signal to an input clock signal to generate a first

control signal, wherein the fifth signal corresponds with an output signal of the first storage

device;

a third multiplexor coupled with the first set of output taps, wherein the third multiplexor

provides a sixth signal to a first interpolator circuit;

a fourth multiplexor coupled with the second set of output taps, wherein the fourth

multiplexor provides a seventh signal to the first interpolator circuit;

a fifth multiplexor coupled with the first set of output taps, wherein the fifth multiplexor

provides an eighth signal to a second interpolator circuit;

a sixth multiplexor coupled with the second set of output taps, wherein the sixth

multiplexor provides a ninth signal to the second interpolator circuit;

wherein the first interpolator provides a tenth signal to a second storage device;

the second interpolator provides an eleventh signal to the second the second

storage device; and

the second storage device provides a twelfth signal that operates as a quadrature

output clock signal; and

a second control circuit that provides a second control signal, a third control signal, a

fourth control signal, and a fifth control signal, respectively, to the third multiplexor, the fourth

multiplexor, the fifth multiplexor, and the sixth multiplexor.

Claim 62 (previously presented) The circuit of claim 61, wherein the first and

second signals are complementary to one another and correspond with a reference clock signal.

Claim 63 (previously presented) The circuit of claim 61, further comprising a flip-

flop for generating a test signal, the flip-flop having a data input terminal coupled with the third

multiplexor to receive the sixth signal and a clock input terminal coupled with the fourth

multiplexor to receive the seventh signal, wherein

the second control circuit receives the first control signal and the test signal and generates

the second control signal and the fifth control signal by offsetting the first control signal by a

selected offset value in a first direction relative to the magnitude of the first control signal and

generates the third control signal and the fourth control signal by offsetting the first control signal

by the selected offset value in a second direction that is opposite to the first direction, where the

selected offset value is selected by starting with a first value and successively changing the

selected offset value until the test signal changes value.

Claim 64 (previously presented) The circuit of claim 61, wherein a rising edge of the

fifth signal, which corresponds to the output signal of the first storage device, corresponds to a

rising edge of the third signal provided by the first multiplexor and a falling edge of the fifth

signal corresponds with a rising edge of the fourth signal provided by the second multiplexor.

(previously presented) The circuit of claim 61, wherein the first and Claim 65

second delay lines each include power control circuitry for selectively powering off one or more

delay elements of the first and second delay lines.

(previously presented) The circuit of claim 65, wherein the power control Claim 66

circuitry powers off the one or more delay elements of the first and second delay lines that are

located subsequent to respective selected output taps of the first and second delay line, wherein

the first and second delay lines comprise sequentially arranged delay elements.

(previously presented) The circuit of claim 66, wherein each of the Claim 67

sequentially arranged delay elements comprises a differential delay circuit having first and

second logic gates having a plurality of inputs where a first input of each of the first and second

logic gates is used to either enable or power off the delay element.

(currently amended) A circuit comprising: Claim 68

a first delay line having a first set of output taps and a first input terminal for receiving a

first signal;

a second delay line having a second set of output taps and a second input terminal for

receiving a second signal;

a first multiplexor coupled to the first set of output taps, the first multiplexor providing a

third signal to a first storage device;

McDonnell Boehnen Hulbert & Berghoff LLP 300 South Wacker Drive Chicago, Illinois 60606

a second multiplexor coupled to the second set of output taps, the second multiplexor

providing a fourth signal to the first storage device;

a control circuit for comparing a fifth signal to an input clock signal to generate a first

control signal, wherein the fifth signal corresponds with an output signal of the first storage

device;

a third multiplexor coupled with the first set of output taps, wherein the third multiplexor

provides a sixth signal to a first interpolator circuit;

a fourth multiplexor coupled with the second set of output taps, wherein the fourth

multiplexor provides a seventh signal to the first interpolator circuit;

a fifth multiplexor coupled with the first set of output taps, wherein the fifth multiplexor

provides an eighth signal to a second interpolator circuit;

a sixth multiplexor coupled with the second set of output taps, wherein the sixth

multiplexor provides a ninth signal to the second interpolator circuit;

wherein the first interpolator provides a tenth signal to a second storage device;

the second interpolator provides an eleventh signal to the second the second

storage device; and

the second storage device provides a twelfth signal that operates as a quadrature

output clock signal;

a second control circuit that provides a second control signal, a third control signal, a

fourth control signal, and a fifth control signal, respectively, to the third multiplexor, the fourth

multiplexor, the fifth multiplexor, and the sixth multiplexor; and

a flip-flop for generating a test signal, the flip-flop having a data input terminal coupled

with the third multiplexor to receive the sixth signal and a clock input terminal coupled with the

fourth multiplexor to receive the seventh signal, wherein

the second control circuit receives the first control signal and the test signal and generates

the second control signal and the fifth control signal by offsetting the first control signal by a

selected offset value in a first direction relative to the magnitude of the first control signal and

generates the third control signal and the fourth control signal by offsetting the first control signal

by the selected offset value in a second direction that is opposite to the first direction, where the

selected offset value is selected by starting with a first value and successively changing the

selected offset value until the test signal changes value.

Claim 69 (previously presented) The circuit of claim 68, wherein the first and

second signals are complementary to one another, the first signal being in-phase with a reference

clock signal and the second signal being out-of-phase with the reference clock signal.

Claim 70 (previously presented) The circuit of claim 68, wherein a rising edge of the

fifth signal, which corresponds to the output signal of the first storage device, corresponds to a

rising edge of the third signal provided by the first multiplexor and a falling edge of the fifth

signal corresponds with a rising edge of the fourth signal provided by the second multiplexor.

Claim 71 (previously presented) The circuit of claim 68, wherein the selected value

is initially set at a predetermined lower limit and successively increased until the test signal

changes value.

Claim 72 (previously presented) The circuit of claim 68, wherein the selected value

is initially set at a predetermined upper limit and successively decreased until the test signal

changes value.

McDonnell Boehnen Hulbert & Berghoff LLP 300 South Wacker Drive Chicago, Illinois 60606 (312) 913-0001